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| Test # | Feature and directed test strategy | Spec Section  # | Priority | Test Sequence | Verification Criteria |
| 1 | Clock frequency and reset | Clock is 50MHz  Reset is active low | high | clk, reset | waveform |
| 2 | Single port RAM | write\_en should be one bit  read\_enb should be one bit | high | write\_enb  read\_enb | constraint c1 { write\_enb != read\_enb ;} |
| 3 | Input values | data\_in should be 8 bit  address should be 5 bit | low | write\_enb  read\_enb  data\_in  address | Class randomize |
| 4 | Reset | Active low reset | high | reset | task t1;  Data\_in = Z  Data\_out = Z  Address =0  Write\_enb = 0  Read\_enb = 0 |
| 5 | Writing data | reset ==1 && write\_enb ==1 | high | reset  write\_enb | task  reset ==1 && write\_enb ==1 -> Data\_in -address |
| 6 | Reading the data | reset ==1 && read\_enb ==1 | high | reset  read\_enb | Task  reset ==1 && read\_enb ==1 ->  Address-Data\_out |
| 7 | Write disable | Address Invalid | mid | reset  write\_enb  address | task  If(reset ==1 &&write\_enb ==1 )  If( !rangeof[address] )  write\_enb = 0; |
| 8 | Read when address is invalid | Data\_out = Z | mid | reset  read\_enb  address | Task  If(Reset ==1 && read\_enb ==1 )  If( !rangeof[address] )  Data\_out = Z |
| 9 | Violation of  Set up and hold time | All the signals must satisfy set up and hold time | high | Clk  reset  Read enable  write enable  data\_in  address | Clocking block  Skew time |
| 10 | Address and data\_in | Cover all the patterns | low | address  Data\_in | randc |
| 11 | Assertion to check correctness for read and write operation | Assertion must be satisfied | mid |  | Assert property-  Reset and en = 1-> read/write  Clk cycle |
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